Modulation Signal Chain for a 5G PDSCH Reciever

[1]Arunakumara, [2]Mrs. DEEPA

[1]M. TECH (VLSI design and Embedded system), Dept. of E & IE, SIT, Tumakuru, India

[2]Assistant Professor, Dept. of E & IE, SIT, Tumakuru, India

[1]arunsonu341@gmail.com [2]rmdeepa@yahoo.com

Abstract

LTE (Long Term Evolution), marketed as 5G LTE, is a standard for wireless communication of high-speed data for mobile phones and data terminals. It increases the system capacity and speed. The standard is developed by the 3GPP (3rd Generation Partnership Project). The scrambling and modulation was implemented using hardware and software methods. The using of scrambling and modulation mapping with help of constellation method is used. Constellation method is easily differentiating the real and imaginary terms of the modulation mapping. Depending on the hardware structure, particular scrambling and modulation mapping was designed using Verilog RTL coding. Simulation and synthesis was carried out using Xilinx Vivado 2015.4.2 design and implemented on Artix-7 FPGA board. Clock cycle delay is reduced to two clock cycles.

Keywords: LTE, PDSCH, Scrambling, Modulation Mapping, Constellation, Verilog RTL, Artix-7.

Introduction

Long Term Evolution (LTE), marketed as 5G LTE, is a standard for wireless communication of high-speed data for mobile phones and data terminals [1]. It increases the system capacity and speed. The standard is developed by the 3GPP [2].

Vivado Design Suite is a Xilinx software suite for synthesizing and analyzing HDL designs that supersedes Xilinx ISE with additional chip development system features and high-level synthesis. Vivado 2015.4.2 represents a ground-up rewriting and rethinking of the entire design flow (as compared to ISE), and reviewers described it as "well-convinced, tightly integrated, fast, scalable, maintainable and intuitive." The Vivado System Edition includes an in-built logic simulator unlike ISE that relied on simulation modalism.

Scrambling is a technique that does not increase the number of bits and causes the problem of synchronization with technique such as Bipolar Alternate Inversion (AMI) is the continuous sequence of zeros creates synchronization problems [3]. This project 16bit data scrambling is used. And the mainly 16bit of Pseudo random data is given through test bench or text files [4]. Scrambling is discussed as shown in figure.3.

Modulation is a process of mixing a signal with a sinusoid to produce a new signal [5]. This new signal, conceivably, will have certain benefits over an un-modulated signal. Mixing of low frequency signal with high frequency carrier signal is called modulation. QPSK, 16QAM 64QAM [6], [7].

The message is then transmitted from the PDSCH and is received by the receiver where a modulation mapping through constellation diagram check is carried out. This process helps to determine the output of the receiver [8]. This entire process is demonstrated using Verilog HDL is a hardware description language used in electronic design automation to implement designs in systems such as field-programmable gate arrays. All the statements are executed concurrently in Verilog.

Simulation results for QPSK, QAM16, QAM64 have been described. All the simulation and synthesis use Xilinx Vivado 2015.4.2 design suite and implemented on Artix-7 FPGA board.

Proposed Transceiver Architecture For High Speed Data Rate

The message from PDSCH channel has to be transmitted. The channel processing steps which are carried out by the PDSCH transmitter blocks are transport block, CRC, LDPC, code block segmentation, and receiver part blocks are code block concatenation, scrambling and modulation mapping blocks achieves increased in speed, high bandwidth and efficiency.

I.Realization of Scrambling

A scrambling is a device and encodes the message signals in the sender side message. Scrambling is used by additional component of random data is generated by software and pseudo random data is generated as shown in below fig.1.

Scrambling is eliminating long sequences of 0's and 1's and avoiding the synchronization problem. The scrambler is replace the sequence into the other sequence without removing the original original data [9].

This project 16bit data scrambling is used. And the mainly 16bit of Pseudo random data is given through test bench or text files [10]. Scrambling is discussed as shown in figure.3. The scrambling is widely used in sattelite, radio rely and wireless communication.

Purpose of scrambling

To avoid the long sequences of bits of same values of 0's and 1's.

The random generator used to a practically feed a random number and which extends the random seed value.

II.Realization of Modulation

Mainly used to modulation mapping the data and control message bits. After the codewords are given to the message bits it need to undergo modulation mapping to generate complex valued of real and imaginary symbols [11]. Signals used for generation of QPSK, QAM16, and QAM64 is shown in TABLE.1.

Table 1. Signals Used For Generation Of Qpsk, Qam16, Qam64

Signals	Description
Clock	Positive edge clock
Reset	Active high reset
Input	input data taken in Selection of modulation
Start	Start signal is High(1) to run the program
Modulation Selector	00 - QPSK 01 - QAM16 10 - QAM64 Otherwise no operation
In-phase	Real term in-phase of output data
Quadrature-phase	imaginary term Quadrature -phase of output data
Output data	(I+jQ) both real and imaginary of output data

The output from the scrambler is fed into the modulation mapper which consist of a multiplexer component to choose the type of modulation required and accordingly the input data is depends on modulation selector for application how much bits is taken choose the selector QPSK, QAM16, QAM64. Depending upon the modulation mapping and imaginary and real value is differentiate in easily is used the constellation diagram method is used [12]. as shown in below fig.1. The constellation diagram is used to modulation mapping with the help of look up table method as shown in below TABLE.2.

Table.2. Constellation Table Of QPSK

Array Index (Input Symbol to QPSK Modulator)	Array Index Represented in Binary	Array value I+JQ (Output of QPSK Modulator)
0	00	1+1j
1	01	-1+1j
2	10	+1-1j
3	11	-1-1j

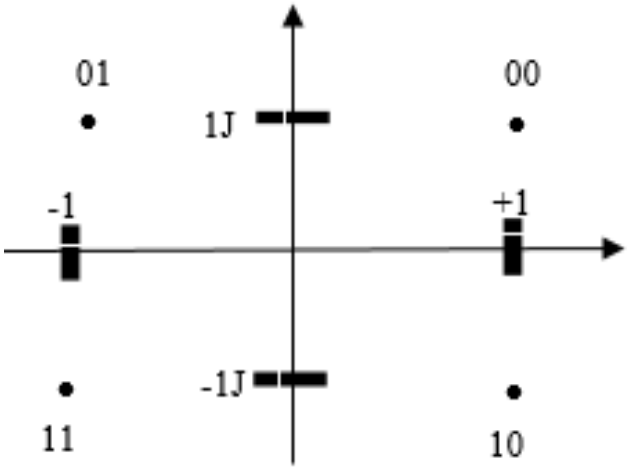

Figure.1. Constellation Diagram of QPSK

Iii. Block Diagram Of Modulation Signal Chain For A 5g Receiver.

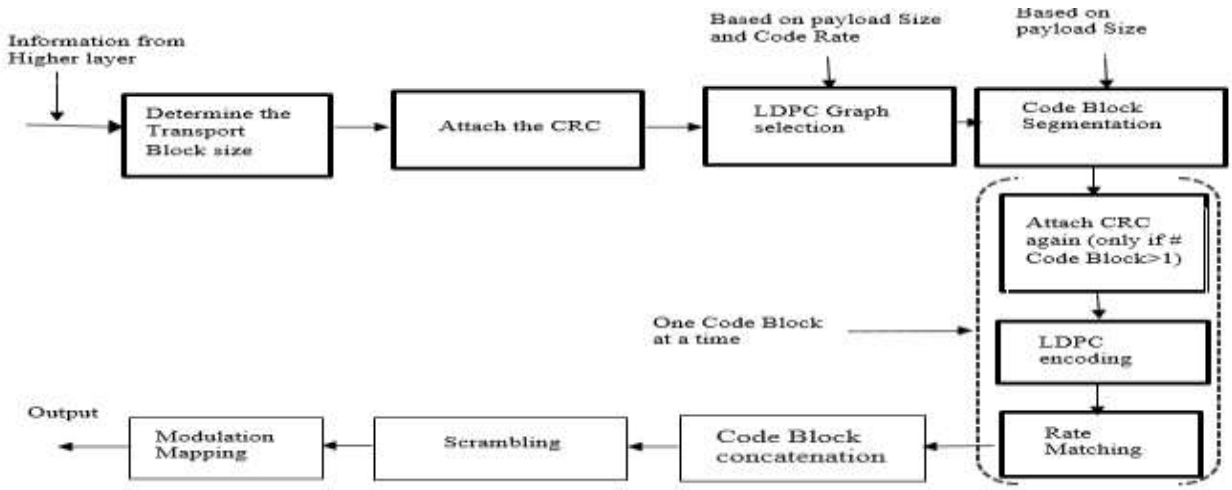

Fig.2. Encoder and Modulator signal chain for a 5G transmit waveform Information bits are received from the higher layer.

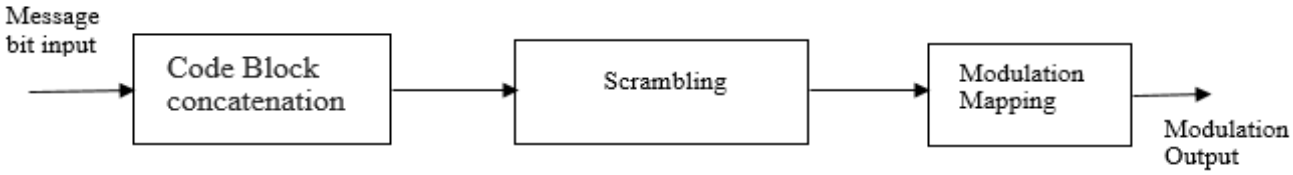

Fig.2. Modulation signal chain for a 5G PDSCH are received from the higher layer.

The transportation block size is determined by the Number of Physical Resource Blocks (NPRB) and the MCS (Modulation and Coding Scheme).

Cyclic Redundancy Check (CRC) is attached to each transportation block that detects errors. A Low-Density Parity Check (LDPC) code in information theory is a linear error correction code

Segmentation of the code block is a generic procedure that is commonly used before encoding turbo. Its main function is to divide a large block of transport into smaller blocks of code.

Rate matching is a very important block in the processing of baseband in PDSCH. The matched output code block at this point rate is concatenated back together. Scrambling is a technique thus avoiding long sequences of bits of the similar value. Modulation is a process of mixing a signal with a sinusoid to produce a new signal. This new signal, conceivably, will have certain benefits over an un-modulated signal.

Results and Discussion

The single word code is scrambled through the generated sequence of pseudo random. In scrambling, adders are replaced by simple xor operation when scrambled sequence is generated. The scrambled sequence is modulated by QPSK and generates complex modulated output. A complex evaluation's modulated output. These are data mapped in the transmitter to their corresponding RE positions. The data will be retrieved, scrambled and mapped on the receiver, code word will be obtained. The output simulations are shown in fig. and fig.3.

The PDSCH downlink transmitter and receiver architecture device utilization summary is shown in fig.2. Three adders and 9 multiplexers are used by the receiver. Taking the delay of the two clock cycle.

The modulation signal chain for a 5G receiver, scrambling and modulation mapping are simulated in Xilinx Vivado 2015.4.2 tool is used and implemented on Artix-7 board.

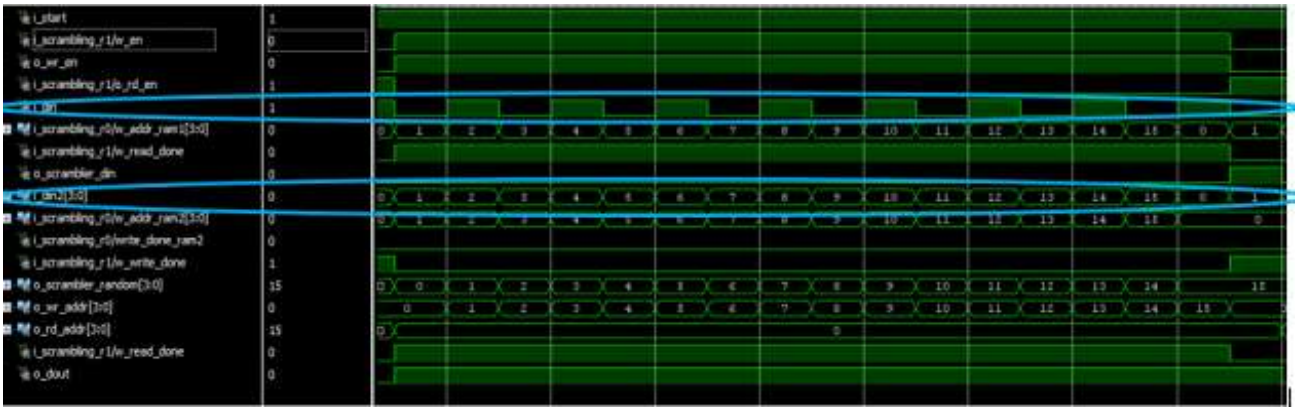

Fig.3. Output waveform of simulation of scrambling write operations.

In scrambling, the input is the i_din and i_random_data of length 16 bits with i_din is 1010011010110101, the i_random_data of another input is 2531096874acbfde… This all are inputs and i_start is high (1), write_enable and i_enable is high (1) the RAM memory is write the data of i_din and i_random_data. Once the write operations are complete write_done is made high (1) and next go to the read operations. The above Fig.3.shows the output waveform of simulation result of scrambling write operations.

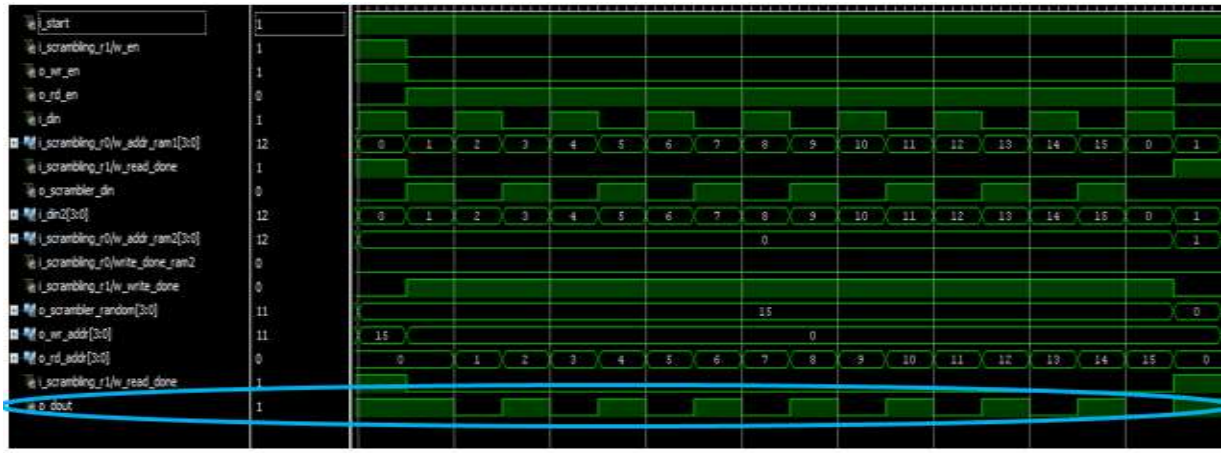

Fig.4. Output waveform of simulation of scrambling write operations.

In scrambling, the input is the i_din and i_random_data of length 16 bits with i_din is 1010011010110101, the i_random_data of another input is 2531096874acbfde… This all are inputs and i_start is high (1), read_enable is high (1) and i_enable is low (0) the RAM memory is read the data of o_dout is 0011001101101011. Once the read operations are complete read_done is made high (1) and next go to the write operations. The above Fig.4.shows the output waveform of simulation result of scrambling read operations.

When modulator selector is '00' QPSK is selected and output waveform for QPSK is as shown in the below Fig.5.

Fig.5. Output waveform of a QPSK Modulation mapping.

When modulator selector is '01' QAM16 is selected and output waveform for QAM16 is as shown in the below Fig.6.

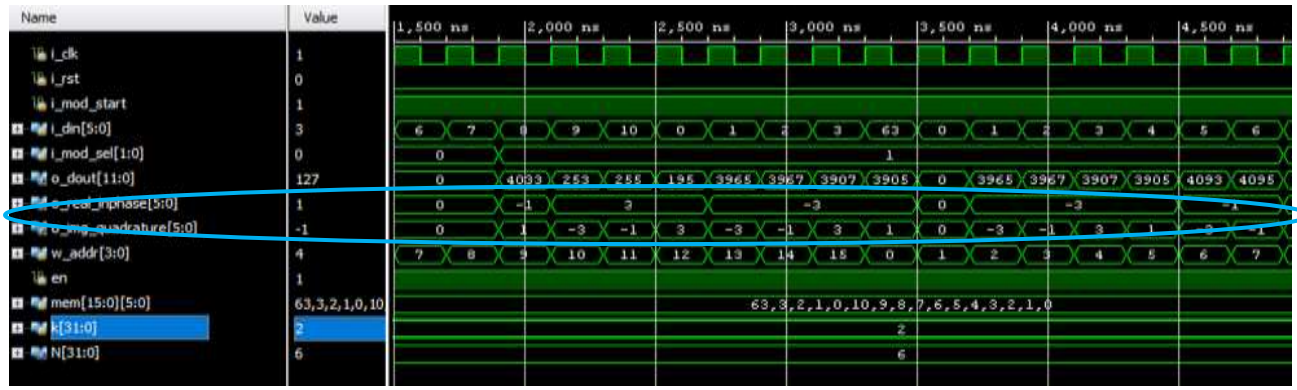

Fig.6. Output waveform of a QAM16 Modulation mapping

When modulator selector is '10' QAM64 is selected and output waveform for QAM64 is as shown in the below Fig.7.

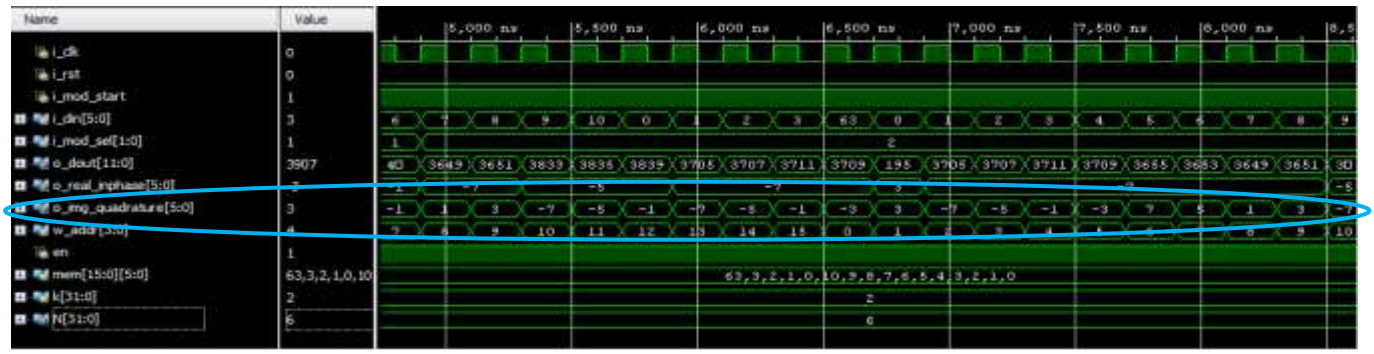

Fig.7. Output waveform of a QAM64 Modulation mapping.

Interfacing diagram of scrambling is as shown in Fig.8.

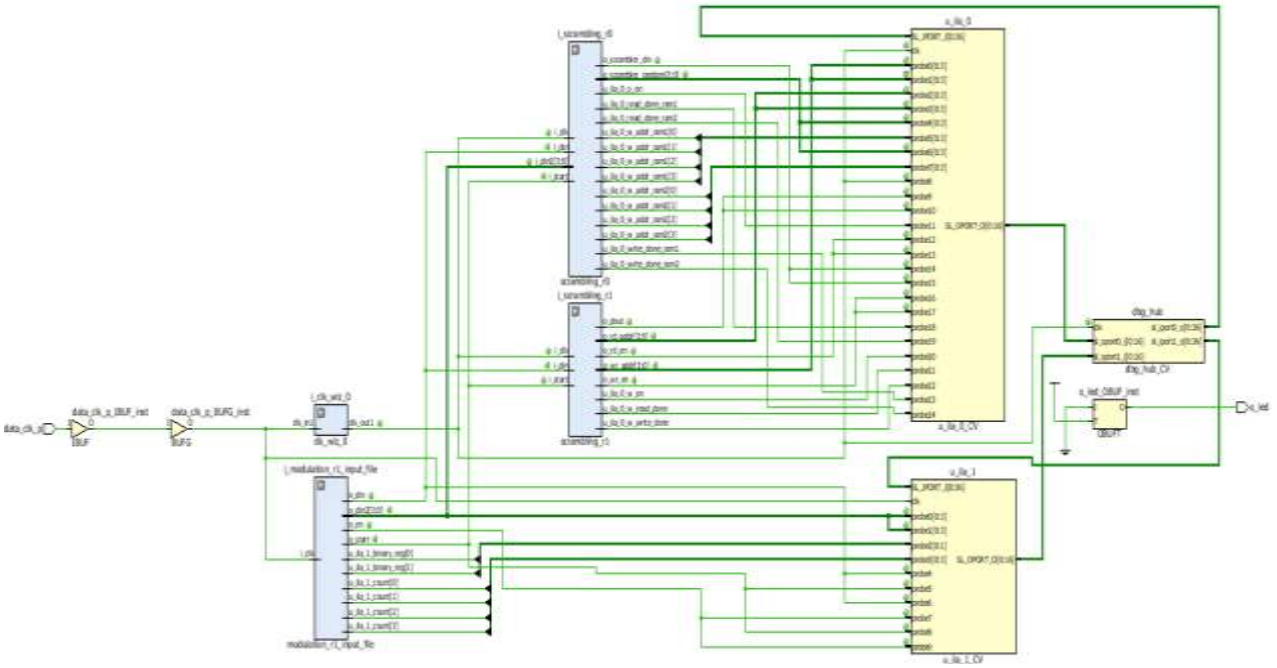

Fig.8. RTL Schematic of scrambling.

Interfacing diagram of modulation mapping is as shown in Fig.9.

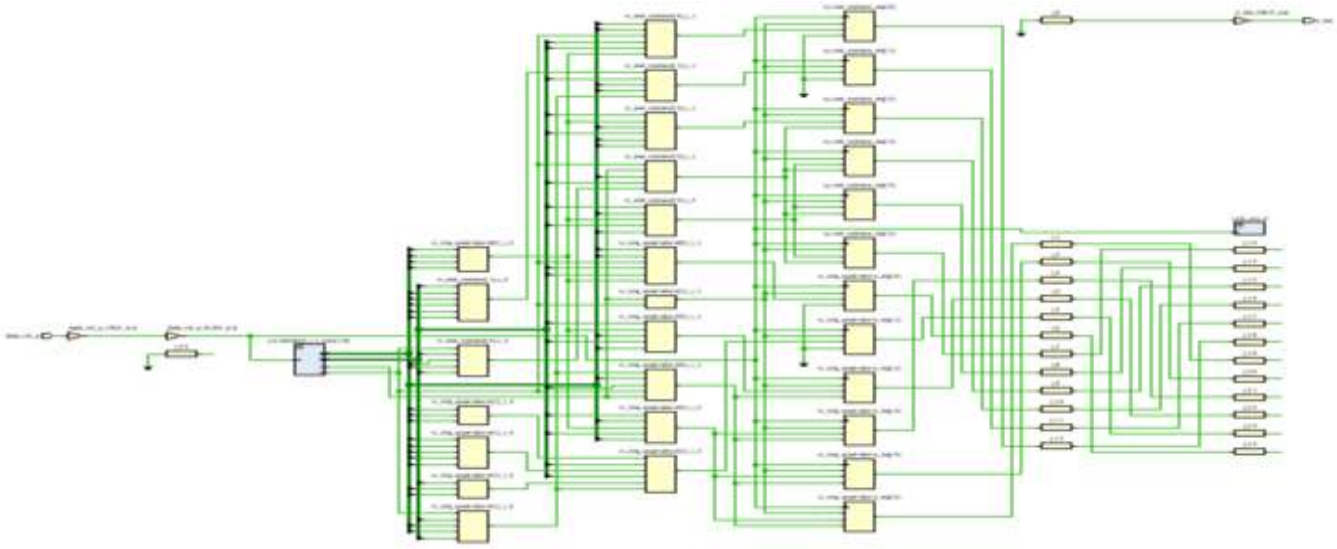

Fig.9. RTL Schematic of modulation mapping.

SYNTHESIS: Scrambling and modulation mapping Verilog HDL Code is then synthesized using the XC7A100TFTG256-1 device with the package of Artix 7 FPGA family implementation and the implementation clock frequency is 10 MHz. The characteristic of the device is listed in Table.2.

Design summary: The design summary consists below reports.

Clock Management: The clock managements are tabulated in Table.3.

Table.3. Clock utilizations report.

Site Type	Used	Fixed	Available	Util%
GLOBAL CLOCK BUFFERs	0	0	624	0.00
BUFGCE	0	0	288	0.00
BUFGCE_DIV	0	0	48	0.00
BUFG_GT	0	0	192	0.00
BUFGCTRL*	0	0	96	0.00
PLLE3_ADV	0	0	24	0.00
MMCME3_ADV	0	0	12	0.00

Some of the key highlights of the clock management architecture include:

- High-speed buffers and routing for low-skew clock distribution.
- Frequency synthesis and phase shifting.
- Low-jitter clock generation and jitter filtering.

Block RAM: The Block RAM is tabulated in Table.4.

Table.4. Block RAM utilizations report.

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	1080	0.00
RAMB36/FIFO*	0	0	1080	0.00
RAMB18	0	0	2160	0.00

Some of the key features of the BRAM include:

- Dual-port 36 Kb BRAM with port widths of up to 72.
- Programmable FIFO logic.
- Built-in optional error correction circuitry.

Input/Output:

The I/O utilization report is tabulated in Table.5.

Site Type	Used	Fixed	Available	Util%
Bonded IOB	0	0	520	0.00
HPIOB	0	0	416	0.00
HRIO	0	0	104	0.00
HPIOBDIFFINBUF	0	0	240	0.00
HPIOBDIFFOUTBUF	0	0	240	0.00
HRIODIFFINBUF	0	0	48	0.00
HRIODIFFOUTBUF	0	0	48	0.00
BITSLICE_CONTROL	0	0	96	0.00
BITSLICE_RX_TX	0	0	624	0.00
BITSLICE_TX	0	0	96	0.00
RIU_OR	0	0	48	0.00

Table.5. Input/output utilizations report.

Some highlights of the input/output functionality include:

- High-frequency decoupling capacitors within the package for enhanced signal integrity.
- Digitally Controlled Impedance that can be 3-stated for lowest power, high-speed I/O operation.

Conclusions

The design on Modulation signal chain for a 5G receiver was implemented using scrambling and modulation mapping. Verilog code was synthesized using Xilinx Vivado 2015.4.2 tool and implemented on Artix-7 FPGA board. Scrambling and QPSK, QAM16 and QAM64 modulation mapping techniques were adopted. To reduce the clock cycle delay of the total two clock cycle delay.

Acknowledgments

We are thankful to Lekha Wireless Solutions Pvt. Ltd. Bangalore for providing all support to carry out the project.

References

1. Yuya Saito, Anass Benjebbour and Yoshihisa Kishiyama, "Spectral Efficiency Improvement with 5G Technologies: Results from Field Tests", IEEE Journal 2016.
2. Ertugrul Basar, "Index Modulation Techniques for 5G Wireless Networks", IEEE Communications Magazine • July 2016.
3. K.G. Digish, "ASIC Implementation of Physical Downlink Shared Channel for LTE", 2014 International Conference on Control, Instrumentation, Communication and Computational Technologies (ICCICCT).
4. S. Syed Ameer Abbas, S. l. Thiruvengadam, M. Punitha, "Realization of PDSCH Transmitter and Receiver Architecture for 3GPP-LTE Advanced", IEEE WiSPNET 2016.
5. Roger piqueras and Jover vuk marojevic, "Security and Protocol Exploit Analysis of the 5G Specifications", January 17, 2019
6. Jeebak Mitra, and Lutz Lampe, "Serial Concatenation of Simple Linear Block Codes and Differential Modulations", IEEE TRANSACTIONS ON WIRELESS COMMUNICATIONS, VOL. 7, NO. 5, MAY 2008
7. Nghi H. Tran, Tho Le-Ngoc, "Achieving Near-Capacity Performance on Multiple-Antenna Channels with a Simple Concatenation Scheme", IEEE TRANSACTIONS ON COMMUNICATIONS, VOL. 58, NO. 4, APRIL 2010.
8. Yan Xin, Ivan J. Fair, "Guided Scrambling Polynomials for Periodic Quotient Relationship Patterns", IEEE TRANSACTIONS ON INFORMATION THEORY, VOL. 54, NO. 3, MARCH 2008.
9. Yung-Chih Tsai, Hao-Hsiang Chung, Mao-Chao Lin, "Scrambling-Based Shaping for Turbo Coded Modulation", IEEE TRANSACTIONS ON COMMUNICATIONS, VOL. 58, NO. 11, NOVEMBER 2010.
10. Kushan B. Vadwala (2014), "Universal Scrambler by using Verilog HDL", Vadwala 3(3): March, 2014.
11. St´ephane Y. Le Goff, Samer S. Al-Samahi, "Selected Mapping without Side Information for PAPR Reduction in OFDM", IEEE TRANSACTIONS ON WIRELESS COMMUNICATIONS, VOL. 8, NO. 7, JULY 2009.

12. Ruey-Yi Wei, "Differential Encoding by a Look-Up Table for Quadrature-Amplitude Modulation", IEEE TRANSACTIONS ON COMMUNICATIONS, VOL. 59, NO. 1, JANUARY 2011.

13. Weichen Xiang, Ste´phane Le Goff, Martin Johnston and Kanapathippillai Cumanan, "Signal Mapping for Bit-Interleaved Coded Modulation Schemes to Achieve Secure Communications", IEEE TRANSACTIONS ON COMMUNICATIONS, VOL 2015.

14. Piya Patcharamaneepakorn, Cheng-Xiang Wang, Mohammed M. Alwakeel, "Quadrature Space-Frequency Index Modulation for Energy-Efficient 5G Wireless Communication Systems", IEEE TRANSACTIONS ON COMMUNICATIONS, 2017.

15. Hassan M. Navazi, Md. Jahangir Hossain, "Efficient Multi-Dimensional Mapping Using QAM Constellations for BICM-ID", IEEE TRANSACTIONS ON WIRELESS COMMUNICATIONS, VOL. SEPTEMBER 2017.

16. Amber Sultan, Xuelin Yang, Adnan A.E.Hajomer, Syed B.Hussian, and Weisheng Hu, "Dynamic QAM Mapping for Physical-Layer Security Using Digital Chaos", Received July 15, 2018, accepted August 17, 2018, date of publication August 23, 2018, date of current version September 21, 2018.